Shelf-Life Evaluation of Lead-Free Component Finishes

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ABSTRACT

The integrated circuit (IC) industry is converting to lead (Pb)-free termination finishes for leadframe-based packages. IC component users need to know the maximum length of time that components can be stored prior to being soldered. This study predicts shelf life of the primary Pb-free finishes being proposed by the industry. Components were exposed to a controlled environment, with known aging acceleration factors. The Pb-free components were exposed to a Battelle Class 2 environment both in and outside of their normal packing materials. Results show that the Pb-free-finished ICs stored in tubes, trays, or tape-and-reel packing material pass solderability testing after 96-h exposure to the Class 2 environment. This exposure correlates to eight years in an uncontrolled indoor environment, such as a warehouse.

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Introduction

This study determines the shelf life of integrated circuit (IC) packages with lead (Pb)-free finishes on their leads or terminations. TI defines “lead (Pb)-free” or “Pb-free” to mean RoHS[1] compatible, including a lead concentration that does not exceed 0.1% of total product weight and, if designed to be soldered, suitable for use in specified lead-free soldering processes.[2] Any product designed to be soldered and designated as Pb-free by TI does not simply utilize a Pb-free finish, but is also suitable for use in high-temperature soldering (250°C/260°C), per the applicable industry standards. Palladium (Pd)-based finishes are the primary Pb-free finishes used for leadframes plated prior to assembly of the IC package.[3,4,5] Pd-based finishes included in this study are nickel/palladium (NiPd), nickel/palladium/gold (NiPdAu), and nickel/palladium/gold/silver (NiPdAu-Ag). Matte tin (Sn) is a Pb-free finish also being proposed as a replacement for tin/lead (SnPb) plating. Components with matte-Sn-finished leads and, as a control, components with SnPb-finished leads are included in this study. The Sn or SnPb finish is plated after molding of the IC package.

An assessment of the shelf life of NiPd-finished components was done in the past by exposure of NiPd-finished components to Battelle Class 2 mixed flowing gas (MFG) conditions. That study showed no degradation of soldering performance after an exposure period that correlated to eight years of shelf storage.[6] In another study, solderability and board-mount testing on NiPd-finished units that had been stored for 51 months showed no degradation in soldering performance of the NiPd-finished units.[7]

This follow-up shelf-life study was prompted by the expanded use of NiPdAu finish, as well as plans for the use of matte-Sn finishes by some IC manufacturers and subcontract assembly/test houses supplying Pb-free packages.

Background

One method used to assess shelf life, as measured by component lead solderability, is to expose the subject devices to a known, controlled atmosphere that accelerates the effects of normal environmental exposure. This is a useful tool if reasonable care is taken to select a test method and conditions so that the time acceleration factor is valid, and the failure mechanisms are consistent with real-world conditions.

Steam conditioning (formerly known as steam aging) of the IC units prior to solderability testing is a common procedure used in the industry. Previous work has shown that when Pd-finish components are steam conditioned, mold resins or other organic residue may be deposited onto the surface of the Pd. Such deposits prevent dissolution of the Pd during solderability testing.[5] The solderability mechanism of NiPd or NiPdAu is dissolution of the Pd (and Au, if present) and wetting the Ni. In contrast, for SnPb- and Sn-finished leads, the soldering mechanism is a fusing (melting) of the Sn or SnPb on the lead and wetting to the Cu base metal. If contaminants from steam conditioning are on the surface of either Sn or SnPb, they float from the finish surface when it melts. This artifact of the steam conditioning process does not correlate with actual storage conditions for NiPd- or NiPdAu-plated leads. Steam conditioning prior to solderability testing has proven to be a nonreproducible method for predicting solderability performance of NiPd and similar nonfusible coatings. For the shelf-life study documented in this report, a conditioning method was used with known acceleration factors and with a mechanism approximating that seen in the real world.

Procedure

To study shelf life by solderability testing of surface-mount ICs, a Battelle Class 2 MFG environment was selected. This test has been well characterized by previous work and represents a slightly corrosive indoor atmosphere where the gas concentrations and humidity levels result in corrosion of plated copper (Cu) materials, but not copper creep corrosion.[8,9] Class 2 environments generally are described as indoor environments having no humidity control, such as that typically found in a warehouse.

This test was conducted in a MFG chamber designed to the schematic shown in Figure 1. The test conditions are shown in Table 1 and are described in detail in ASTM B827–92.[9]

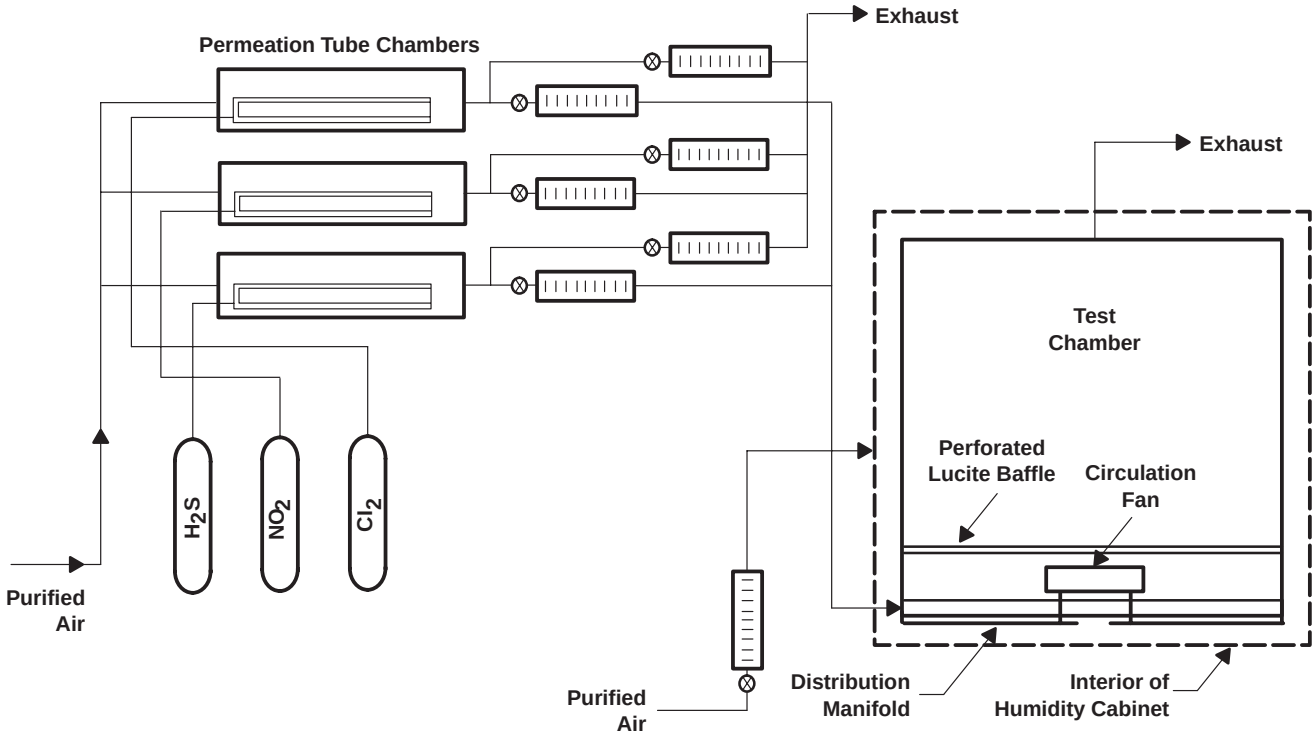

Figure 1. Schematic of MFG Chamber

Table 1. Battelle Class 2 MFG Test Conditions

TEST CONDITION	RANGE
Cl_2 concentration	10 ± 3 ppb
NO_2 concentration	200 ± 50 ppb
H_2S concentration	10 ± 5 ppb
Relative humidity	70 + 3%/− 0%
Temperature	30 ± 2°C
Chamber volume change	3 to 6 times per hour
Acceleration factor	400−1000

It is important to include standard reactivity coupons along with the test specimens. Measurement of mass gain on the coupons confirms that proper test conditions were achieved and facilitates verification of acceleration factors.[11]

Subject surface-mount IC devices, with the various finishes (see Table 2), were placed in the chamber, both unprotected and partially protected from the gas flow. Unprotected samples were totally exposed to the MFG environment, i.e., placed in an open petri dish. Additional samples from the same lots were left in the typical (opened) packing used in product shipment. SOICs were left in shipping tubes and in tape-and-reel packing materials. None of the parts were in hermetic anti-static bags or cardboard shipping/packing boxes when tested. The minimum specified thickness and vacuum X-ray fluorescence thickness measurements of samples from each of the Pd-based lots are shown in Table 3. No thickness measurements were done on the Sn and SnPb lots that were obtained from commercial sources.

The attenuation effect of the packing materials (tubes and trays) was significant. Abbott (of Battelle) has stated that the attenuation by packing materials is perhaps the major reason that electronic components can perform reliably in field environments.[12] Virtually any type of packing provides some degree of environmental attenuation compared to free-surface exposure. One could speculate that the corrosion kinetics are controlled by Fick's third law, because the reactive species are in the gas phase, and gas concentration at the metal surface controls the corrosion rate. This can be contrasted with the steam conditioning mechanism, which seems not to mimic storage conditions for Pd-based Pb-free finishes.

Device samples and reactivity coupons were removed from the chamber at 24, 48, 72, and 96 h. Visual microscopic examination was used to grade the effects of the gas exposure, followed by solderability testing. Mass gain measurements of the reactivity coupons confirmed reaction rates and established the appropriate acceleration factor.

Table 2. Component Evaluation

GROUP NO.	PACKAGE	FINISH	PACKING	READ POINT	
				0 h	96 h
1A	20-pin SOIC	NiPdAu 0.01-µm (0.4-µ") Pd	Loose		X
1B			Tube	X	X
1C			Tape		X
2A	20-pin SOIC	NiPdAu 0.02-µm (0.8-µ") Pd	Loose		X
2B			Tube	X	X
2C			Tape		X
3A	20-pin SOIC	NiPd	Loose		X
3B			Tube	X	X
3C			Tape		X
4A	16-pin SOIC	Matte Sn	Loose		X
4B			Tube	X	X
4C			Tape		X
5A	16-pin SOIC	SnPb	Loose		X
5B			Tube	X	X
5C			Tape		X
6A	16-pin SOIC	NiPdAu-Ag	Loose		X
6B			Tube	X	X
6C			Tape		X

Table 3. Ni, Pd, and Au Thickness Measurements

GROUP NO.	PACKAGE	FINISH	METAL	THICKNESS		STANDARD DEVIATION
				MIN SPECIFIED	MEAN	
1	20-pin SOIC	NiPdAu 0.01-µm (0.4-µ") Pd	Ni	0.5 µm (20 µ")	0.64 µm (25 µ")	0.02
			Pd	0.01 µm (0.4 µ")	0.01 µm (0.4 µ")	0.0005
			Au	0.003 µm (30 Å)	0.0035 µm (35 Å)	1.2
2	20-pin SOIC	NiPdAu 0.02-µm (0.8-µ") Pd	Ni	0.5 µm (20 µ")	0.61 µm (24 µ")	0.05
			Pd	0.02 µm (0.8-µ")	0.026 µm (1 µ")	0.003
			Au	0.003 µm (30 Å)	0.0036 µm (36 Å)	1.0
3	20-pin SOIC	NiPd	Ni	1.0 µm (40 µ")	1.10 µm (44 µ")	0.066
			Pd	0.075 µm (3 µ")	0.100 µm (4 µ")	01
			Au	NA	NA	NA
6	16-pin SOIC	NiPdAu-Ag	Ni	0.10 µm (4 µ")	0.75 µm (30 µ")	0.047
			Pd	0.02 µm (0.8 µ")	0.036 µm (1.4 µ")	0.002
			Au (Ag)	0.003 µm (30 Å)	0.0043 µm (43 Å)	0.045

Assessment Methods and Results

Visual Examination

Parts from each of the matrix cells were examined under a microscope at up to 40× magnification. The parts were graded subjectively as to the amount of corrosion products seen on the lead surfaces. An arbitrary scale of 0 to 5 was used, with 0 indicating no corrosion and 5 indicating severe corrosion. Only the loose parts showed corrosion. None approached level 5. The Ag-bearing samples showed relatively more corrosion, likely from the Ag/S tarnish reaction. For subsequent solderability testing, only the 0- and 96-h specimens were tested. A summary of the visual-inspection results for all samples is shown in Table 4.

Table 4. Visual-Inspection Results

GROUP NO.	DESCRIPTION	PACKING	0 h	24 h	48 h	72 h	96 h
1A	NiPdAu − 0.01-µm (0.4-µ") Pd	Loose	0	2	2	2	2.5
1B	NiPdAu − 0.01-µm (0.4-µ") Pd	Tube	0	0	0	0	0
1C	NiPdAu − 0.01-µm (0.4-µ") Pd	Tape	0	0	0	0	0
2A	NiPdAu − 0.02-µm (0.8-µ") Pd	Loose	0	1	2	2	2
2B	NiPdAu − 0.02-µm (0.8-µ") Pd	Tube	0	0	0	0	0
2C	NiPdAu − 0.02-µm (0.8-µ") Pd	Tape	0	0	0	0	0
3A	NiPd − SL-spot Pd	Loose	0	0	1	1	1
3B	NiPd − SL-spot Pd	Tube	0	0	0	0	0
3C	NiPd − SL-spot Pd	Tape	0	0	0	0	0
4A	Matte Sn	Loose	0	0	0	0	0
4B	Matte Sn	Tube	0	0	0	0	0
4C	Matte Sn	Tape	0	0	0	0	NA(1)
5A	SnPb	Loose	0	0	0	0	0
5B	SnPb	Tube	0	0	0	0	0
5C	SnPb	Tape	0	0	0	0	NA(1)
6A	NiPdAu-Ag – Revision 2	Loose	0	3	3	4	3.5
6B	NiPdAu-Ag – Revision 2	Tube	0	0	0	0	0
6C	NiPdAu-Ag – Revision 2	Tape	0	0	0	0	0

(1) NA = not available

Surface-Mount Solderability Test

Solderability of the components was judged with the surface-mount process simulation test method per IPC/EIA/JEDEC J−STD−002B, test method S.[13] This test simulates the reflow environment during surface-mount device board mounting. Testing has shown that this method is more appropriate for surface-mount devices than the traditional dip-and-look method. The results for the surface-mount process simulation test method are shown in Table 5. There were no failures for any of the units tested.

Table 5. Solderability Test Results

GROUP NO.	B (0 h, TUBE)(1)	A (96 h, LOOSE)(1)	B (96 h, TUBE)(1)	C (96 h, TAPE)(1)
1	2/0	5/0	5/0	5/0
2	2/0	5/0	5/0	5/0
3	1/0	5/0	5/0	5/0
4	2/0	5/0	5/0	5/0
5	2/0	5/0	5/0	5/0
6	3/0	5/0	5/0	5/0

(1) Sample size/number of failures

The accept/reject criteria in J-STD-002B is “all leads shall exhibit a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination.” For the surface-mount packages tested, the critical area is defined as the underside of the leads, plus both sides of the leads up to 1× the lead thickness.

Corrosion Products Analysis

The corrosion products on the surface of representative parts were analyzed by SEM/EDAX and Auger. This was done for the control samples (0 h) and for the most heavily corroded parts (96 h). Micrographs are shown in Figures 2–9. The level of corrosion on the loose parts in the petri dishes is evident. Auger analysis of the corrosion deposits confirmed that the predominant species are oxides and chlorides of Cu, with a minor amount of Cu sulfides present. These results are consistent with the nature of corrosion products produced by the gases in the Battelle Class 2 environment. That the surface-mount solderability tests showed no failures indicates that the deposits are quite thin and easily removed by the flux system in the solder paste.

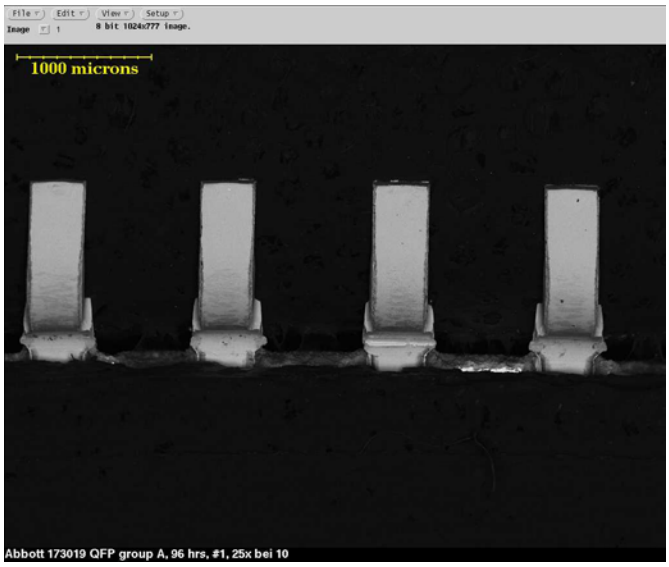

Figure 2. Group 1A NiPdAu 0.01-μm (0.4-μ”) Pd, Loose, 96 h, 25×, Bottom Lead View

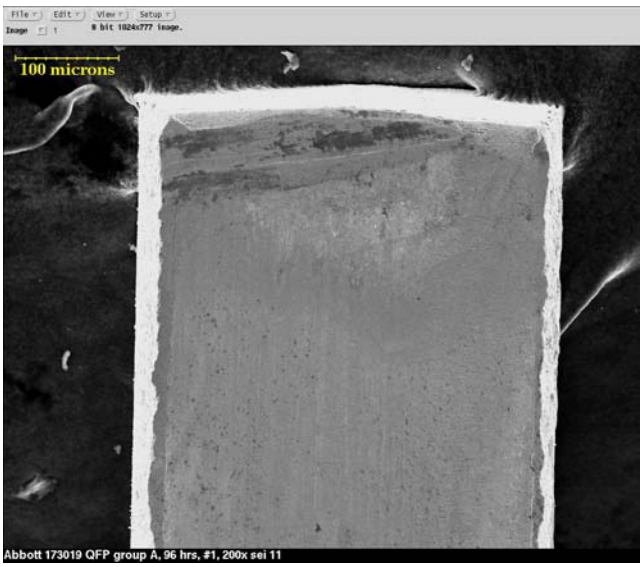

Figure 3. Group 1A NiPdAu 0.01-μm (0.4-μ”) Pd, Loose, 96 h, 200×

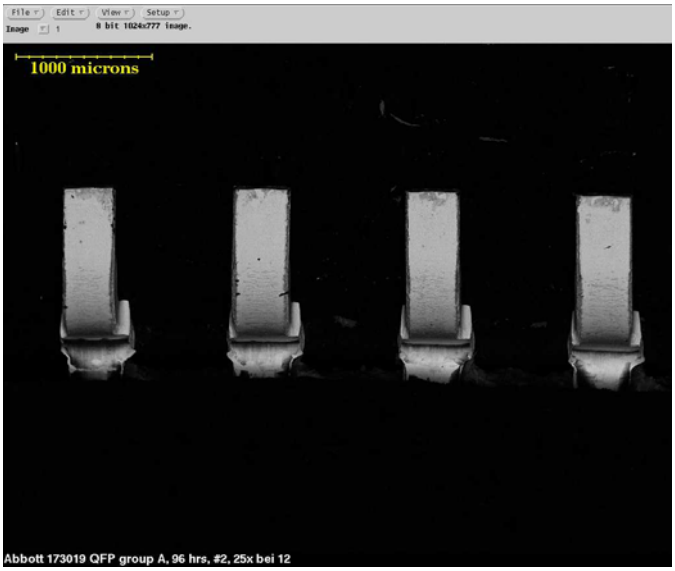

Figure 4. Group 2A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 25×

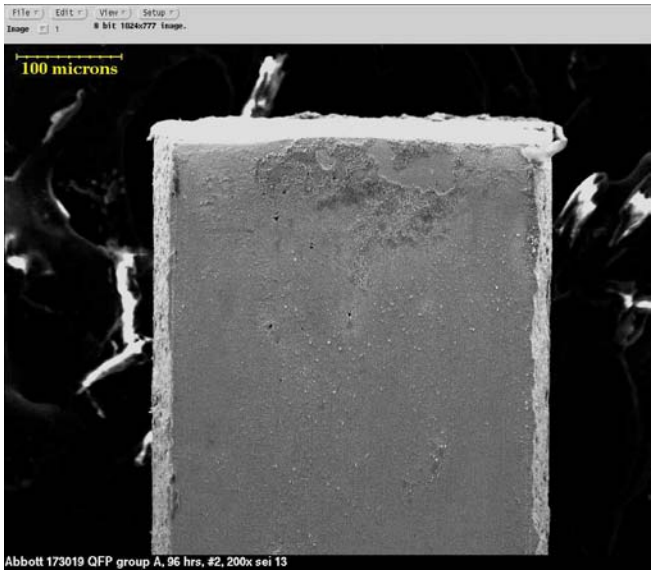

Figure 5. Group 2A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 200×

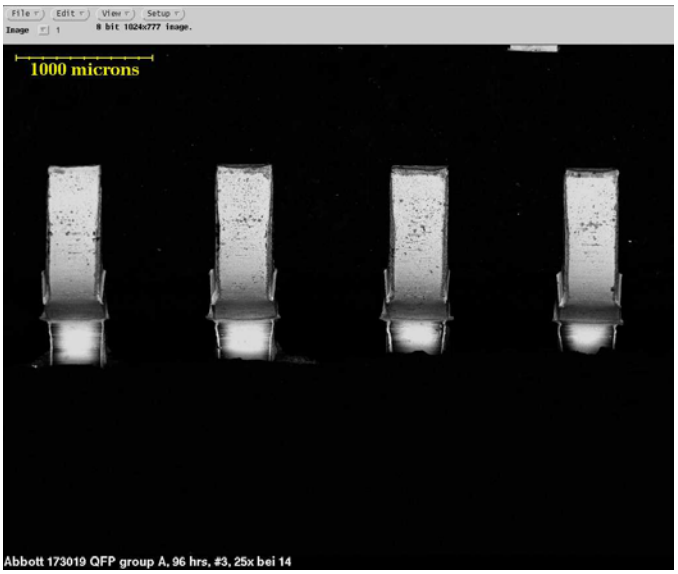

Figure 6. Group 3A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 25×

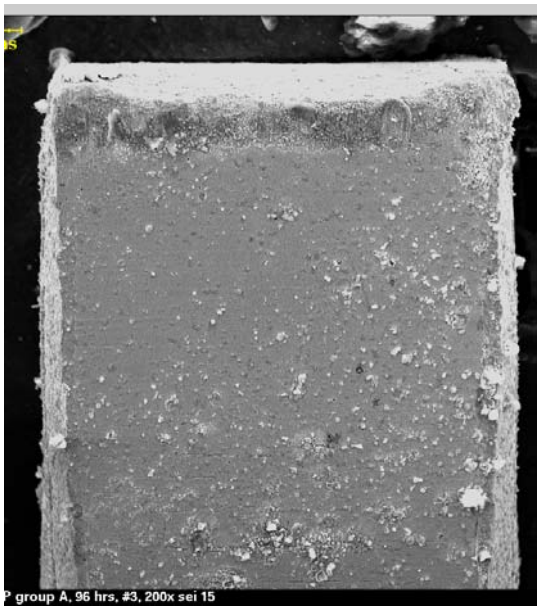

Figure 7. Group 3A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 200×

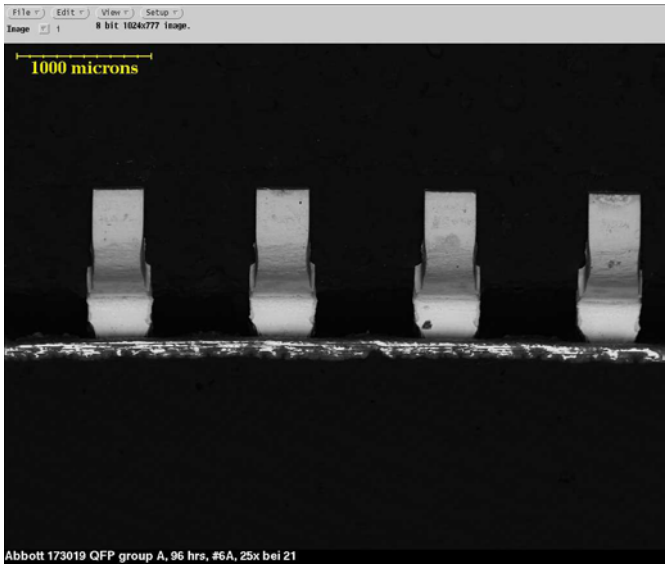

Figure 8. Group 6A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 25×

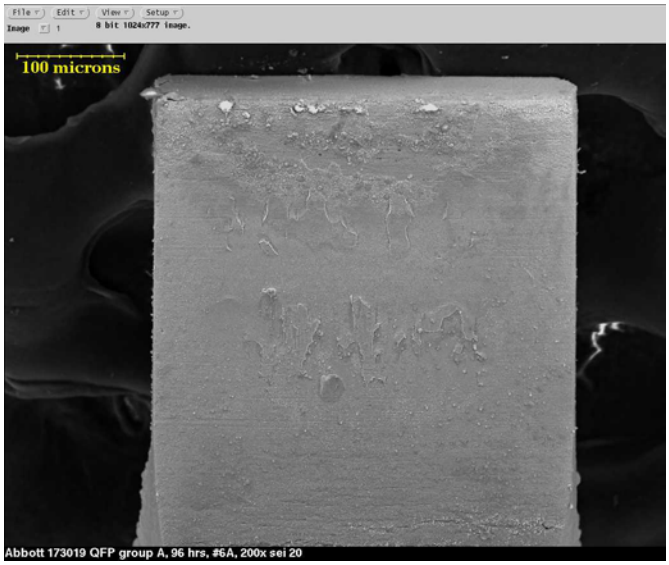

Figure 9. Group 6A NiPdAu 0.02-μm (0.8-μ") Pd, Loose, 96 h, 200×

Auger also confirmed that the Cu-bearing compound deposits seen in the micrographs are thin. Twenty seconds of sputtering was sufficient to bring the surface composition of an area with corrosion products to that of a corrosion-free area. (This thickness is roughly equivalent to sputtering 0.0012 μm (12 Å) of tantalum oxide.)

Wetting-Balance Results

Soldering performance of the component leads was evaluated for each group using the wetting balance. Table 6 shows the time-to-cross-zero axis in seconds for each group. If a sample did not wet (cross the zero axis) during the 10 s of test time, the sample is marked as DNW. In some cases (marked NA), measurement issues impacted the ability to get a reading. The corrosion attenuation effects of the packing materials can be seen in the wetting-balance results. With the NiPdAu versions, non-wetting was seen on units exposed to 96 h in the MFG environment when the units were exposed loose or outside of normal packing materials. However, units exposed to the same test conditions show very short (good) wetting times when the units were exposed to the MFG conditions while in normal packing materials (tube or tape and reel).

Table 6. Wetting-Balance Results (Time to Wet in Seconds)

GROUP NO.	PACKAGE	FINISH	PACKING	READ POINT	
				0 h	96 h
1A	20-pin SOIC	NiPdAu 0.01-µm (0.4-µ") Pd	Loose		DNW
1B			Tube	0.46	0.48
1C			Tape		0.66
2A	20-pin SOIC	NiPdAu 0.02-µm (0.8-µ") Pd	Loose		DNW
2B			Tube	0.57	NA
2C			Tape		0.59
3A	20-pin SOIC	NiPd	Loose		5
3B			Tube	2.43	NA
3C			Tape		0.54
4A	16-pin SOIC	Matte Sn	Loose		1.1
4B			Tube	0.29	0.9
4C			Tape		0.83
5A	16-pin SOIC	SnPb	Loose		0.7
5B			Tube	0.11	0.38
5C			Tape		0.68
6A	16-pin SOIC	NiPdAu-Ag	Loose		DNW
6B			Tube	NA	0.32
6C			Tape		0.22

Board Mount

Units from each group were soldered to PWBs after 0- and 96-h exposure. Appearance of the board-mount solder joints was documented, and lead pull was performed to judge the mechanical strength of the solder joint. Cross sections were taken for each group to determine the solder wetting performance to the underside of the lead.

The no-clean solder paste used for board mount was a commercially available Pb-free alloy with composition of 95.5Sn/4Ag/0.5Cu. Reflow profiles used are shown in Figures 10 and 11.

The board-mount performance (Figures 12–23) was very good for all groups, including the units that were stored outside of packing materials.

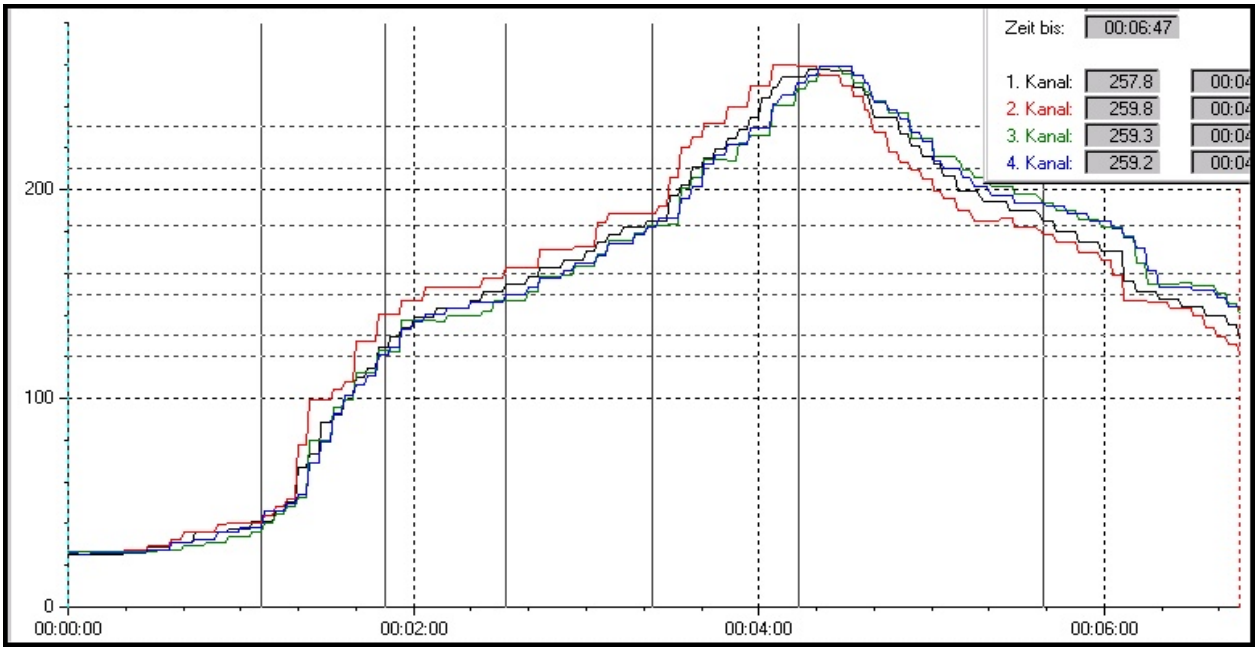

Figure 10. Reflow Profile Used for 20-Pin SOIC Units

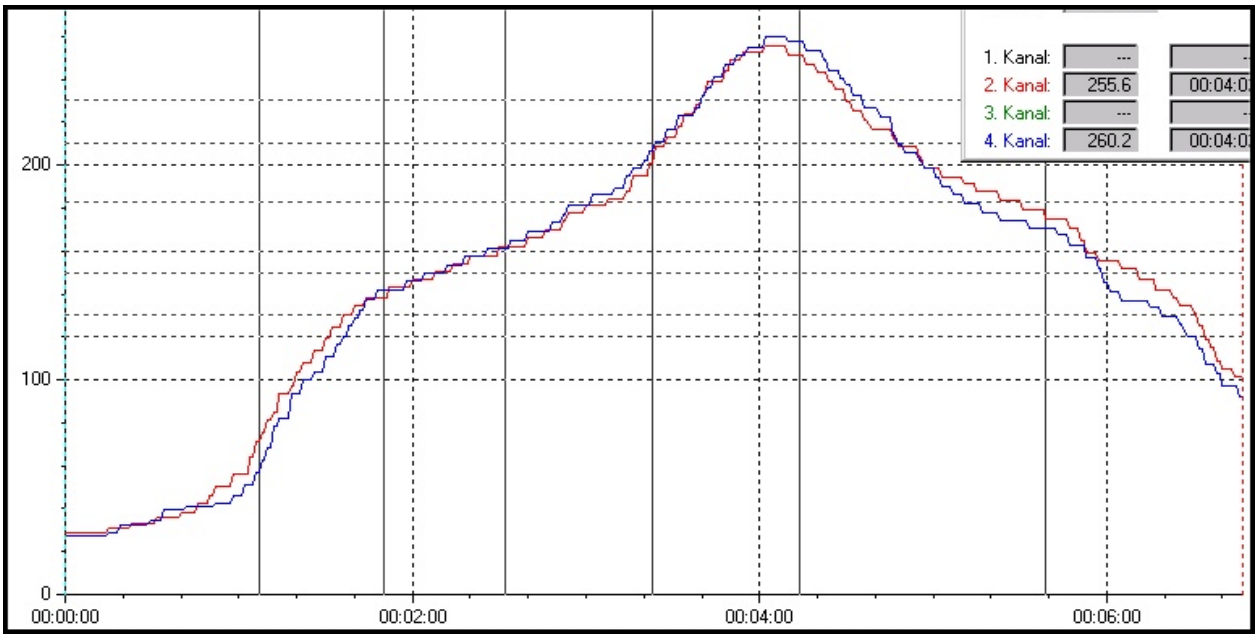

Figure 11. Reflow Profile Used for 16-Pin SOIC Units

Visual Appearance of Solder Joints

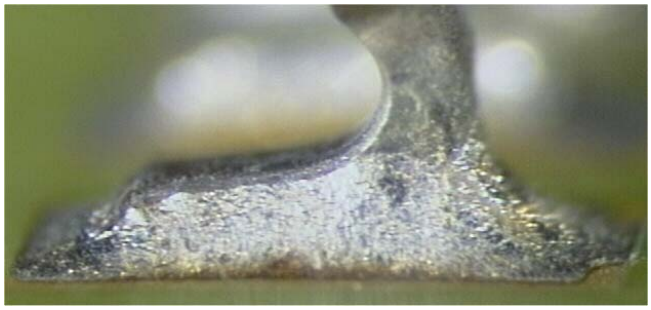

Figure 12. Group 1A, NiPdAu Finish, Stored Loose, 96-h Exposure

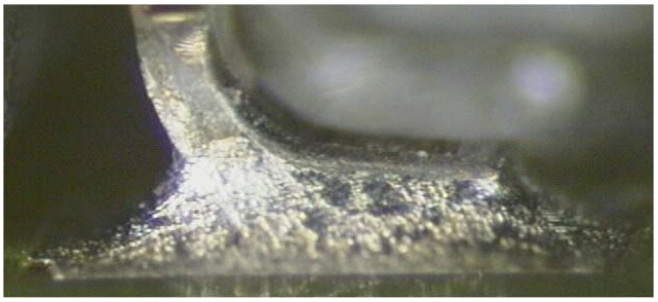

Figure 13. Group 1B, NiPdAu Finish, Stored in Tubes, 96-h Exposure

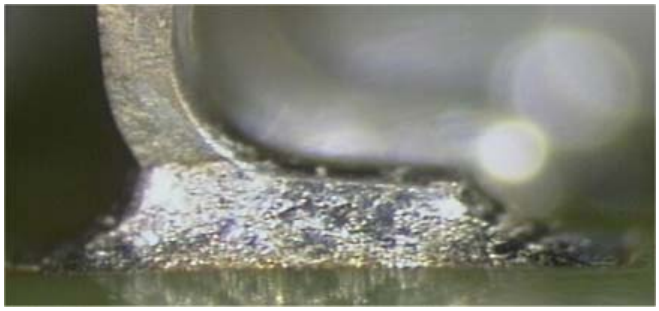

Figure 14. Group 2A, NiPdAu Finish, Stored Loose, 96-h Exposure

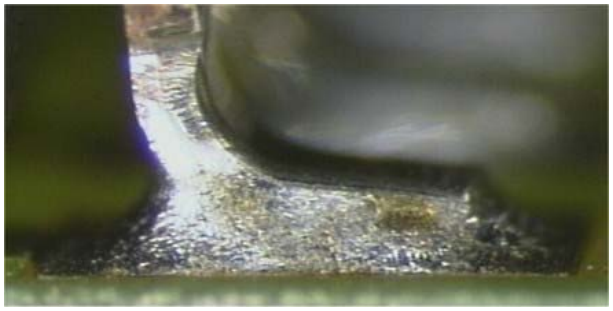

Figure 15. Group 2B, NiPdAu Finish, Stored in Tubes, 96-h Exposure

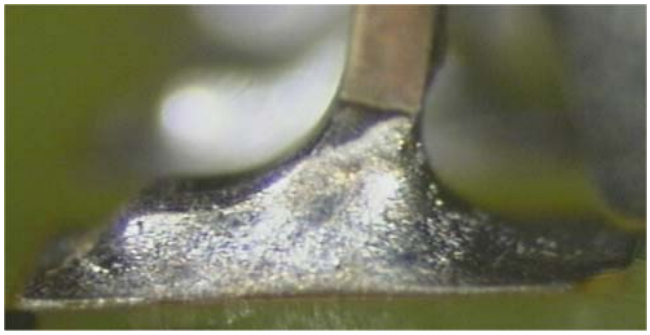

Figure 16. Group 3A, NiPd Finish, Stored Loose, 96-h Exposure

Figure 17. Group 3B, NiPd Finish, Stored in Tubes, 96-h Exposure

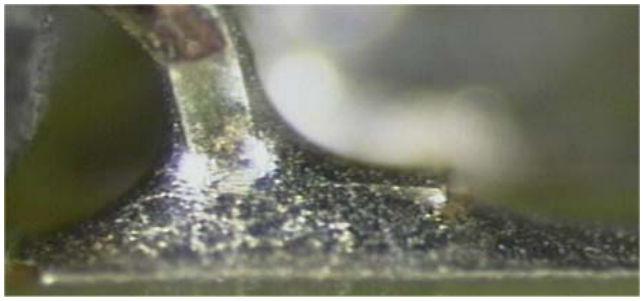

Figure 18. Group 4A, Sn Finish, Stored Loose, 96-h Exposure

Figure 19. Group 4B, Sn Finish, Stored in Tubes, 96-h Exposure

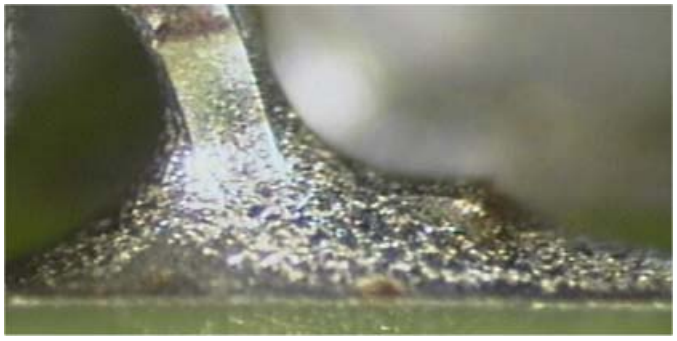

Figure 20. Group 5A, SnPb Finish, Stored Loose, 96-h Exposure

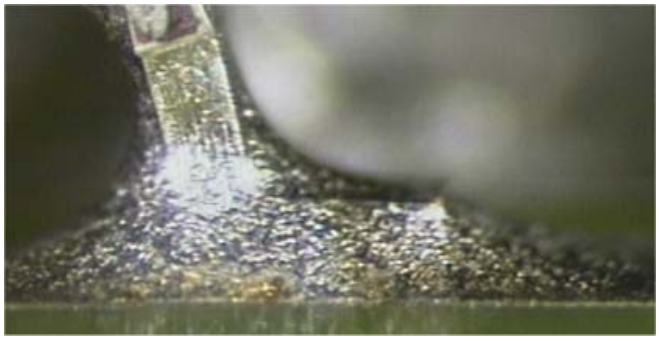

Figure 21. Group 5B, SnPb Finish, Stored in Tubes, 96-h Exposure

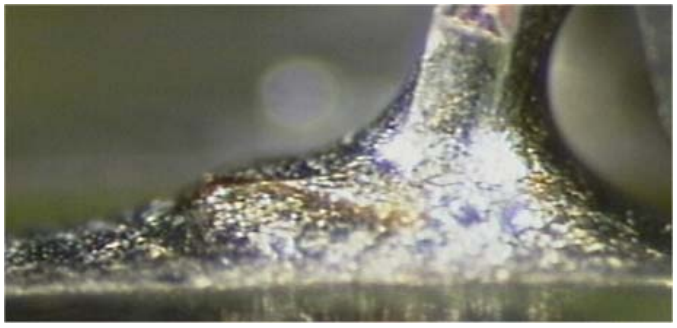

Figure 22. Group 6A, NiPdAu-Ag Finish, Stored Loose, 96-h Exposure

Figure 23. Group 6B, NiPdAu-Ag Finish, Stored in Tubes, 96-h Exposure

All groups exhibited good solder wetting. For all groups (1–6), all units exhibited good solder wetting performance after 96-h exposure, regardless of whether the units were stored loose or in tubes. The visual appearance of all solder joints pass when judged, based on criteria in J-STD-001.[14]

Cross Sections of Solder Joints

For all groups, all units exhibited good solder wetting performance, based on cross sections, after 96-h exposure, regardless of whether the units were stored loose or in tubes. The cross sections of all solder joints pass, when judged based on criteria in J-STD-001 (see Figures 24–35).[14]

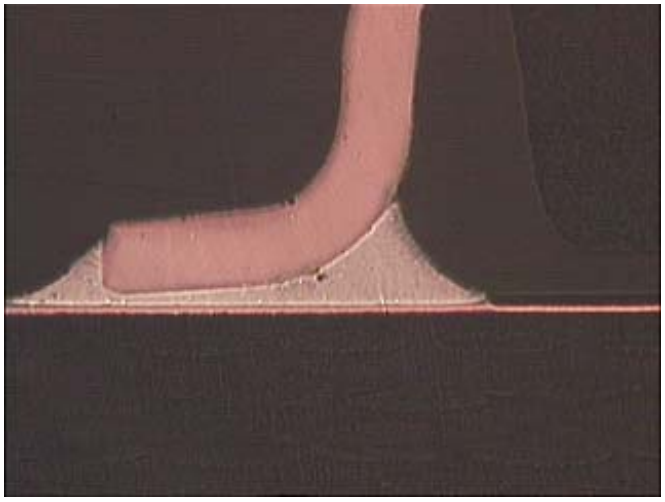

Figure 24. Group 1A, NiPdAu Finish, Stored Loose, 96-h Exposure

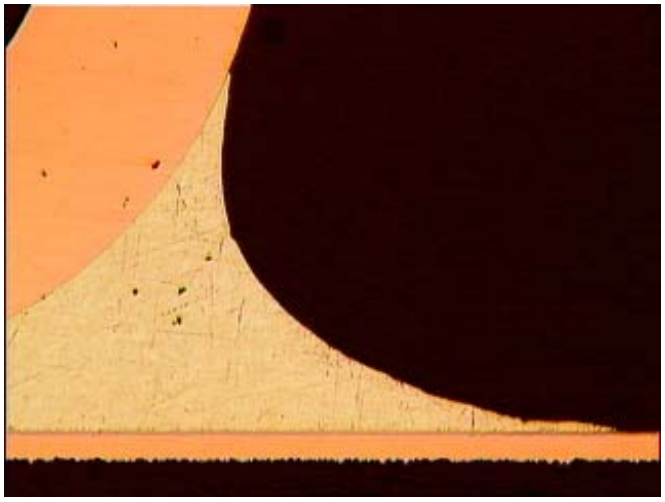

Figure 25. Group 1B, NiPdAu Finish, Stored in Tubes, 96-h Exposure

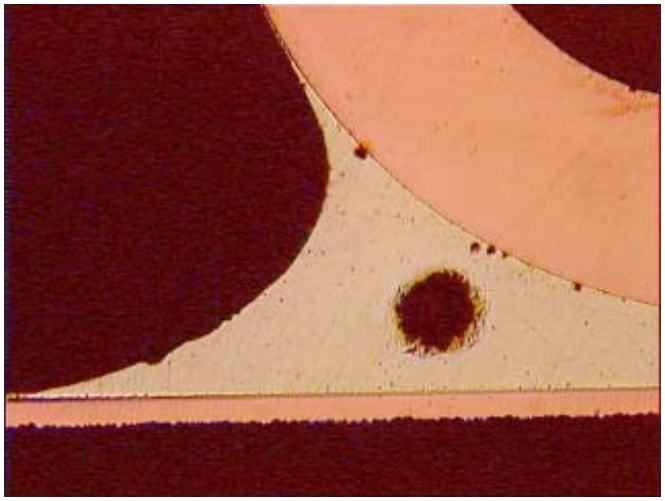

Figure 26. Group 2A, NiPdAu Finish, Stored Loose, 96-h Exposure

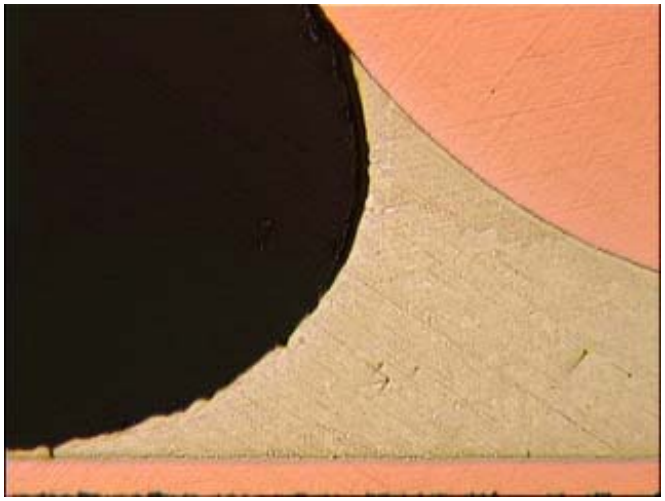

Figure 27. Group 2B, NiPdAu Finish, Stored in Tubes, 96-h Exposure

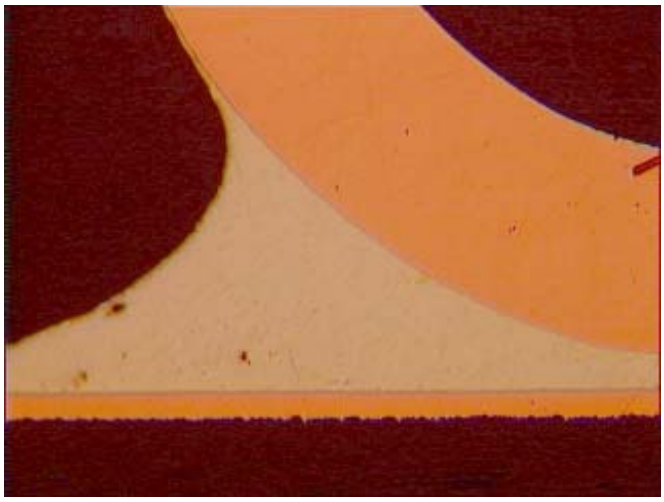

Figure 28. Group 3A, NiPd Finish, Stored Loose, 96-h Exposure

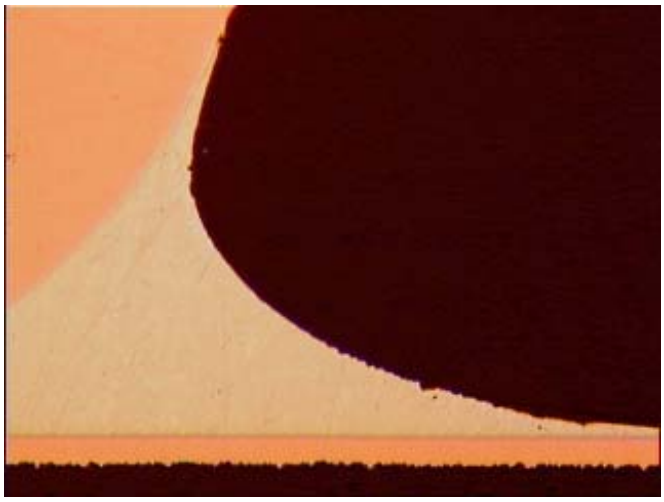

Figure 29. Group 3B, NiPd Finish, Stored in Tubes, 96-h Exposure

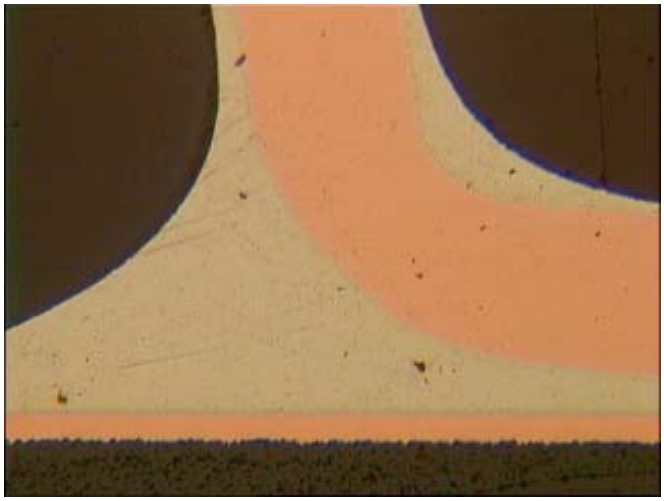

Figure 30. Group 4A, Sn Finish, Stored Loose, 96-h Exposure

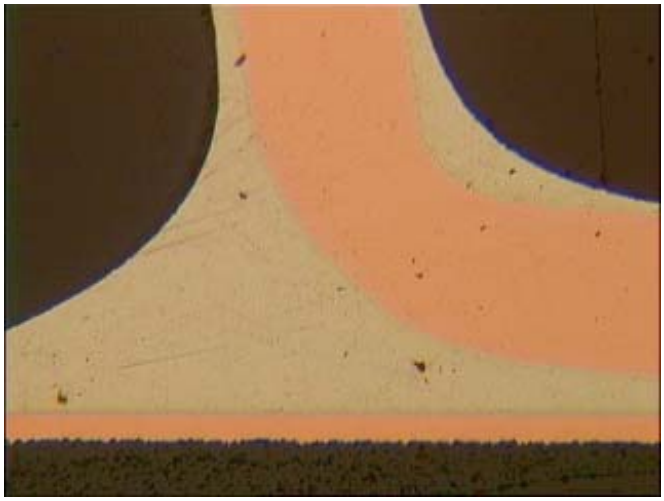

Figure 31. Group 4B, Sn Finish, Stored in Tubes, 96-h Exposure

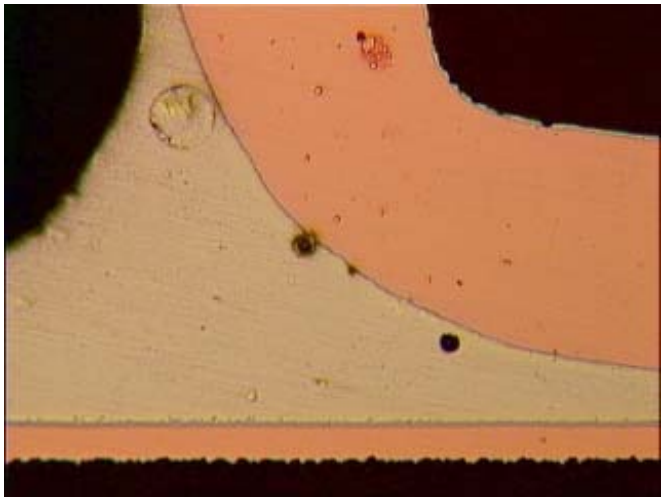

Figure 32. Group 5A, SnPb Finish, Stored Loose, 96-h Exposure

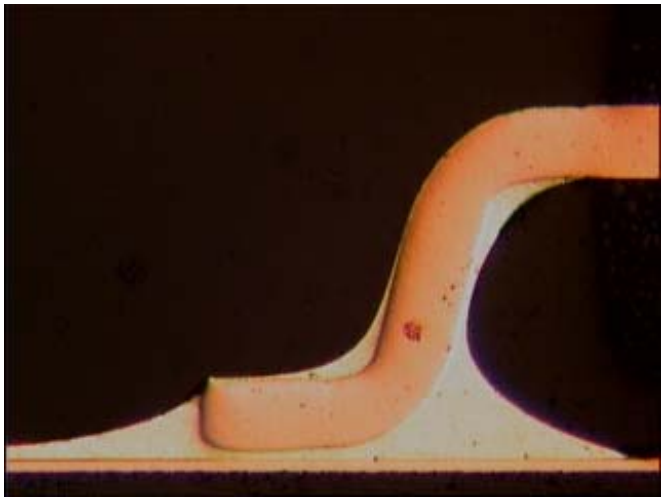

Figure 33. Group 5B, SnPb Finish, Stored in Tubes, 96-h Exposure

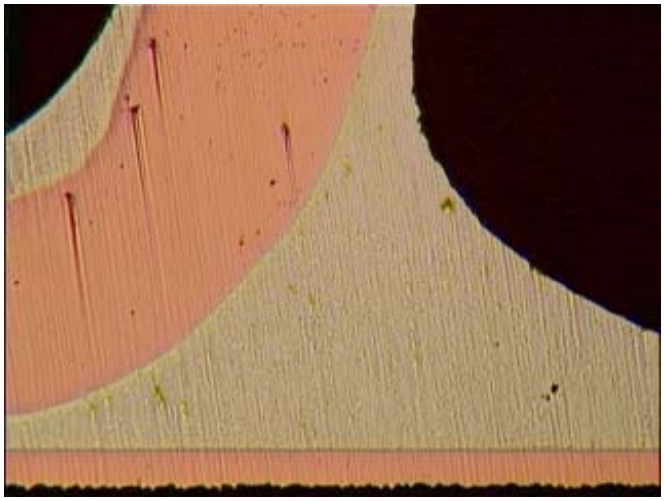

Figure 34. Group 6A, NiPdAu-Ag Finish, Stored Loose, 96-h Exposure

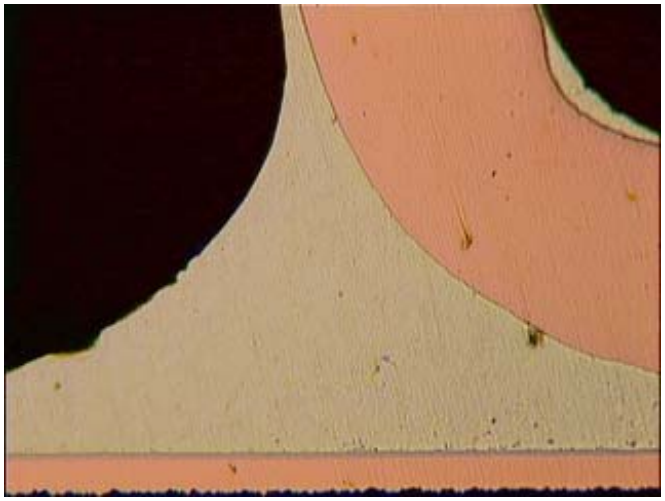

Figure 35. Group 6B, NiPdAu-Ag Finish, Stored in Tubes, 96-h Exposure

Lead Pull

Lead-pull testing determined the force needed to pull an individual IC lead from the PWB land pattern after soldering. First, to allow access to an individual lead on the PWB, the leads were cut near the package body. Next, with the leads separated from the package body, the PWB was fastened in a test fixture. Finally, the lead was pulled perpendicular to the PWB surface until it separated from the PWB. The rate of movement of the test device was 0.4 mm/s vertically to the board surface. Sample size for each group was ten leads. The force needed to pull the lead from the PWB was measured and recorded.

Figure 36 shows lead-pull data for the NiPdAu and NiPd finished components (groups 1−3), while Figure 37 shows lead-pull data for the matte Sn, SnPb, and NiPdAu-Ag components (groups 4−6). Results show essentially equivalent lead-pull values for each lead finish. The minimum lead-pull value specified by industry standards for non-temperature-cycled samples, with the lead cross-sectional area of the units tested, is 10 N.[15] All lead-pull values are above the minimum requirement. Also, note that lead-pull values basically are the same for units board mounted after 0- and 96-h exposure to the MFG environment, independent of whether the units were exposed loose (outside of normal packing materials) or while stored in standard packing materials.

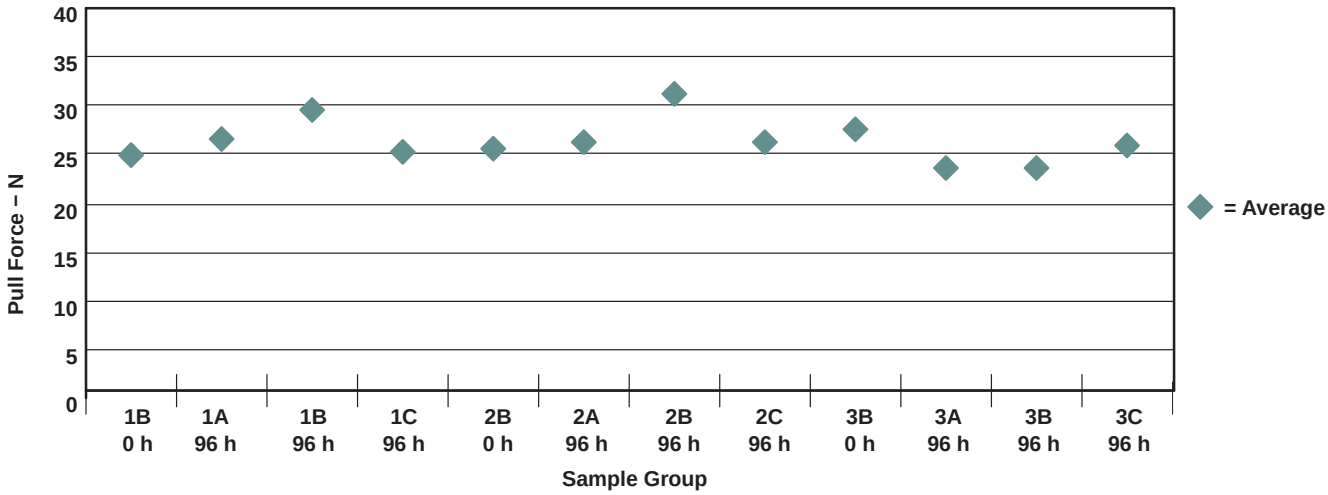

Figure 36. Average Lead-Pull Force for Sample Groups 1–3

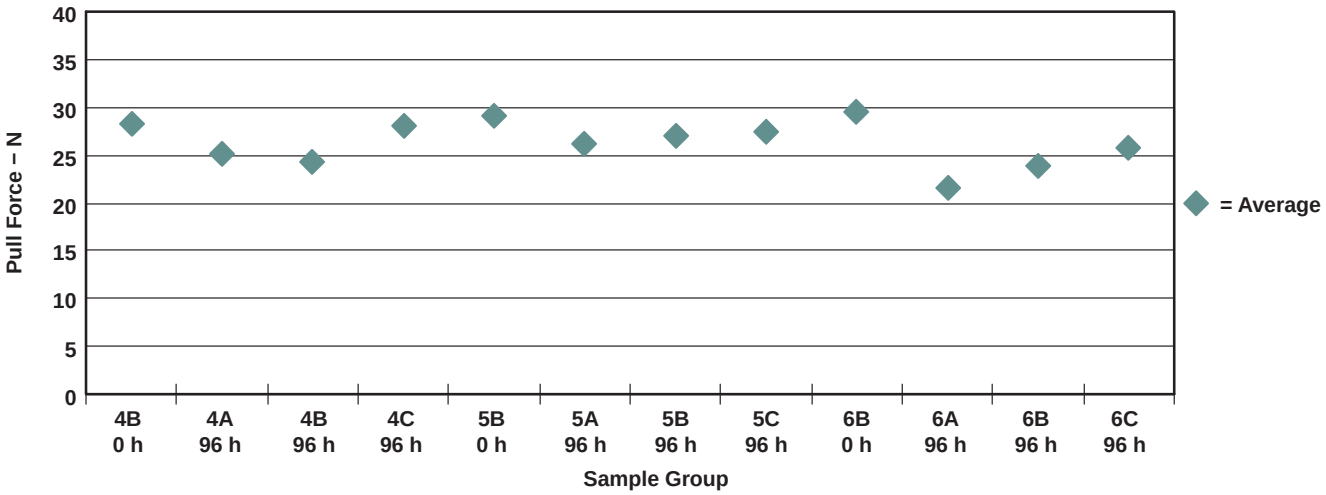

Figure 37. Average Lead-Pull Force for Sample Groups 4–6

Summary of Results

- Visual inspection at up to 40× showed distinguishable corrosion differences among specimens that were loose in petri dishes during the exposure intervals of 0, 24, 48, 72, and 96 h to the Battelle Class 2 environment. Specimens that were exposed while in tubes or tape and reel showed no visible corrosion (see Table 4).
- The surface-mount solderability test, JEDEC J-STD-002, showed no failures for any specimens tested after 96-h exposure to the Battelle Class 2 environment, regardless if they were loose, in tubes, or in tape and reel (see Table 5).
- SEM/EDX analysis and Auger analysis showed thin corrosion films composed primarily of oxides and chlorides of Cu. This is consistent with SEM/EDX found in the prior shelf-life study.[4]
- Wetting-balance data confirms a thin film of corrosion on the loose, 96-h NiPd- and NiPdAu-based finishes. These samples did not wet (DNW) in 10 s. The specimens that were exposed in tubes and in tape and reel for 96 h showed insignificant increases in wetting times.
- Visual inspection of the solder joints for board-mounted, 96-h, loose specimens showed that all solder joints passed J-STD-001.
- The cross sections of the board-mount solder joints all showed good wetting.
- Lead-pull values essentially are the same for units board mounted after 0- and 96-h exposure to the MFG environment, regardless of whether the units were exposed loose or while stored in standard packing materials.

Conclusion

The shelf life of integrated circuits with NiPdAu, NiPd, NiPdAu-Ag, matte Sn, and SnPb-finished leads is >8 years, as measured by solderability after exposure to a Battelle Class 2 MFG environment. Class 2 environments generally are described as indoor environments having no humidity control, such as those found in a warehouse. The results for the NiPd finish duplicate those found previously.[6]

The attenuation effects of IC shipment packaging (tube and tape and reel) is again demonstrated with virtually no corrosion seen on parts that were in such packaging while exposed to 96 h of the Class 2 environment.

Parts that were exposed directly to the Class 2 environment, i.e., in petri dishes, showed visual signs of corrosion that were substantiated by SEM/EDX and by wetting-balance results. However, even with visible thin films of corrosion, these parts easily passed surface-mount solderability testing and related board-mount testing — visual, cross section, and lead pull.

Acknowledgments

The authors wish to recognize the following individuals for their professional assistance:

- Albert Haage and Thomas Refeld of Texas Instruments, Germany for board mounting, wetting balance, and lead-pull testing
- Dr. Al Hopkins of Texas Instruments, Attleboro, S&C Group for SEM/EDX and Auger work

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